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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,627	08/28/2001	Ki Yong Jeon	P-0251	4513

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EXAMINER	
HEINRICHS, CHRISTOPHER P	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,627	JEON	
	Examiner	Art Unit	
	Christopher P. Heinrichs	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/28/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 10-16* is/are rejected.

7)☒ Claim(s) *5 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not include the notary's signature, or the notary's signature is in the wrong place.

It does not include the notary's seal and venue.

Drawings

2. The drawings are objected to because fig. 4, item 33 reads "READ POINTER GENERATING UNIT" but is referred to in the specification as "read pointer controlling unit 33" (page 9, paragraphs 31 and 32) and states that the read pointer generating unit is not shown. The description of object 33 in the specification will be considered but clarification is necessary. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

a. "VC mapping unit 42,..." on page 7 in the last line of paragraph 27 should read "VC mapping unit 43,..."

b. "VC1 framer 34" on page 9 in line 4 of paragraph 33 should read "VC1 framer 35".

c. The "read pointer controlling unit 35" of paragraph 9 line 3 should read "read pointer controlling unit 33".

Appropriate correction is required.

Claim Objections

4. Claim 13 is objected to because of the following informalities: "method of mapping serial data mapping" should read "method of mapping serial data" or "method of serial data mapping". Appropriate correction is required.

5. Claims 2, 4, 9, and 11 are objected to because of the following informalities: they refer to a read pointer generating unit and a read pointer controlling unit. It is believed that the two terms are used interchangeably to refer to a single element. Appropriate correction is required.

6. Claims 5 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 4 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 4 recites the limitation "the read pointer generating unit" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 4 will be considered without the stated limitation.

10. Claim 14 states that the system clock controls the reading of the parallel data unit from the plurality of buffers to the virtual container signal and does not state the necessity of multiplexing the parallel data unit as described in claim 13. This creates confusion as to whether the parallel data unit needs to be multiplexed into the virtual container or if it can be simply read directly into the virtual container.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 3, 6-8, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent #6,285,673 to Blackburn et al.

13. Regarding claim 1, Blackburn discloses a serial data mapping apparatus (delivery unit 10, fig 1) comprising an STM-1 address generating unit (OBC 126, fig 29 item 126, see col 29 lines 3-5) that generates a mapping address (J0/Z0 field, col 29 lines 3-8), a VC mapping unit (MUX/DEMUX 291, FIG 29) that maps a DS asynchronous signal (DS0 data bit serial) to a VC signal (STS-1 SPE) as a byte unit

(byte serial data stream, col 30 lines 37-39), according to the mapping address and an STM-1 formatter (OTM 102, figs 1, 28) that pointer processes and multiplexes a virtual container of the mapped VC signal (see col 27 lines 21 –24) and generates an STM-1 signal (STS-3, fig 28).

14. With regard to claim 3, Blackburn discloses all aspects of the invention of claim 1. Blackburn further discloses a plurality of elastic buffers (fig 29 item 292 is a subsystem of fig 1 item 103 and fig 1 shows a plurality of units 103) that write the DS asynchronous signal as a bit unit (fig 29 shows item 292 writes the bit serial data to the VC mapping unit) and read the DS asynchronous signal as the byte unit (DS0 data byte serial), the plurality of elastic buffers being synchronized to a system clock signal (local time base, fig 29 item 124).

15. Regarding claim 6, Blackburn discloses a serial data mapping apparatus MUX/DEMUX, fig 30 and 29 item 291) comprising a plurality of elastic buffers (DS-1 framer stage 2, fig 30 item 305), each buffer receiving serial asynchronous data (DS0 data) and outputting parallel data bits of the asynchronous data (28 DS1 signals, col 30 lines 58-60) and a virtual container mapping unit (VT1.5 PATH TERM, fig 30 item 306) that receives the parallel data bits from the plurality of elastic buffers and maps the parallel data bits to a virtual container signal (STS-1 SPE, fig 30).

16. With regard to claim 7, Blackburn discloses an STM-1 formatter (OTM, fig 28 item 102) that multiplexes the virtual container signal (STS-1 SPE, fig 30) as an STM-1 signal (STS-3, fig 28).

17. With regard to claim 8, Blackburn further discloses an STM-1 address generating unit (OBC, fig 28 item 126) that generates a mapping address (J0/Z0 field, col 29 lines 3-8), a virtual container multiplexer (DSIMX7, fig 30, within VT1.5 PATH TERM) within the virtual container mapping unit, that multiplexes a number of the parallel data bits received from the plurality of elastic buffers into the virtual container, and a virtual container framer (DS) that identifies a mapping position of the asynchronous signal (STS-1 SPE, fig 30, where the SPE is a VT1.5 mapped SPE), based on the mapping address generated by the STM-1 address generating unit, and controls the multiplexing of the number of parallel data bits into the virtual container (the multiplexing of bits is received and controlled as described in col 29 line 47 – col 30 line 8).

18. Regarding claim 13, Blackburn discloses a method of mapping serial data, comprising: receiving each of a plurality of serial asynchronous data signals into a plurality of elastic buffers (DS0 data and DS1 framer stage 2, item 305 fig 30), respectively; multiplexing parallel data units (28 DS1 signals, col 30 lines 58-60) read from the plurality of elastic buffers into a virtual container signal (STS-1 SPE, fig 30), each parallel data unit containing multiple data bits read in parallel (28 DS1 signals parallel to each other come with clocks so each is serial hence they contain multiple

data bits, see col 30 lines 58-60); and generating an STM-1 (STS-3, fig 28) signal from the virtual container signal.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claims 2, 4, 10-12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent #6,285,673 to Blackburn et al. in view of Figs. 1 and 2 of specification of instant claim.

22. With regard to claim 2, Blackburn discloses all aspects of the invention of claim 1. Blackburn further discloses the plurality of elastic buffers (DS1 FRAMER STAGE 2, fig 30) that write the DS asynchronous signal as a bit unit and read the DS

asynchronous signal as the byte unit (DS0 component byte elements of DS1) but does not specifically disclose the other elements of claim 2. However, figure 2 of the specification teaches a write pointer generating unit that generates write addresses for a buffer (25), a read pointer controlling unit that generates read addresses for a buffer (26), a VC1 mapper (23) that multiplexes parallel asynchronous data of the byte unit into the VC signal according to a format controlling signal, and a VC1 (24) framer that identifies a mapping position of the DS asynchronous signal, according to the mapping address (J1) outputted from the STM-1 address generating unit (fig. 1 item 15), and controls (via "ien" signal) read pointer controlling unit, the elastic buffers (via the read pointer generating unit), and the VC1 mapper according to the identified mapping position. It would have been obvious to one ordinarily skilled in the art at the time of the invention to combine the subsystem description of the VC mapping unit disclosed in the background art with the serial data mapping apparatus disclosed by Blackburn to arrive at the invention of claim 2. The motivation to do so would have been to utilize the plurality of elastic buffers within one VC mapping unit taught by Blackburn in combination with the one write address generating unit and one read pointer controlling unit of the prior art so as to limit the number of gates of the system.

23. With regard to claim 4, the aspects of the invention of claim 2 are set forth above. Figure 2 further discloses that the read pointer controlling unit outputs a start bit (:0) of the byte unit (5:) as the read address (RA).

24. With regard to claim 10, Blackburn discloses all aspects of the apparatus of claim 6. Blackburn further discloses a system clock (LOCAL TIME BASE, fig 29 item 124) that controls the timing of writing the asynchronous data (EGRESS BUS written into buffer, fig 29) and reading the parallel (DS0 DATA BYTE SERIAL read out of buffer, the 8 parallel serial channels constituting the data byte serial signal, fig 29) data bits from a buffer (BIF 125), but fails to disclose using the system clock in conjunction with the plurality of elastic buffers of the VC mapping unit. However, it would have been obvious to one ordinarily skilled in the art at the time of the invention to use the system clock of fig 29 to control synchronized reading and writing of the data to and from the plurality of elastic buffers of claim 6 to arrive at the invention of claim 10. The motivation to do so would have been to solve the problem of jitter described in paragraph 13 of the Background section of the instant application.

25. With regard to claim 11, Blackburn discloses all aspects of the invention of claim 6. Blackburn further discloses an STM-1 formatter (OTM, fig 28 item 102) that multiplexes the virtual container signal (STS-1 SPE, fig 30) as an STM-1 signal (STS-3, fig 28), yet another virtual container mapping unit (VT1.5 PATH TERM, fig 30) that maps portions of the plurality of DS-1 and DS-1E signals (DS0 channels, col 32 lines 2-3) into the virtual container signal, and the STM-1 formatter (as above) that multiplexes the virtual container (STS-1 SPE, fig 30) having the portions of the DS-1 and DS-1E signals into the STM-1 signal. Blackburn fails to disclose the read pointer generating unit. However, Fig. 2 discloses the read pointer generating unit. It would have been

obvious to one ordinarily skilled in the art at the time of the invention to combine the read pointer generating unit disclosed by the prior art with the apparatus disclosed by Blackburn in claim 6 and the VC mapping unit further disclosed by Blackburn to arrive at the invention of claim 11. The motivation to do so would have been to utilize the plurality of elastic buffers within one VC mapping unit taught by Blackburn in combination with the one read pointer generating unit of the system of the prior art, so as to limit the number of gates of the system.

26. With regard to claim 12, Blackburn and the prior art disclose the invention of claim 11. Blackburn further discloses a system clock (LOCAL TIME BASE, fig 29 item 124) that controls the timing of writing the asynchronous data (EGRESS BUS, fig 29) and reading the parallel (DS0 DATA BYTE SERIAL, fig 29) data bits from a buffer (BIF 125), but fails to disclose using the system clock in conjunction with the plurality of elastic buffers of the VC mapping unit. However, it would have been obvious to one ordinarily skilled in the art at the time of the invention to use the system clock in conjunction with the system taught by Blackburn that includes the plurality of buffers to control synchronized reading and writing of the of the plurality of DS-1 and DS-1E signals and writing of the portions of the plurality of DS-1 and DS-1E signals to the virtual container mapping unit to arrive at the invention of claim 12. The motivation to do so would have been to solve the problem of jitter described in paragraph 13 of the Background section of the instant application.

27. Claims 15 and 16 are method claims corresponding to apparatus claim 2, and therefore, are rejected under the same reason set forth in the rejection of claim 2. Apparatus described by claim 2 has only one read pointer generating unit and has only one write pointer generating unit, yet a plurality of elastic buffers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Heinrichs whose telephone number is 571-272-8397. The examiner can normally be reached on Monday through Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER 4/4/05